

REMARKS

Claims 1-6 are the claims currently pending in the Application.

Formal Matters

Applicant thanks the Examiner for acknowledging the claim for foreign priority and the receipt of the priority document.

The Examiner states that for the references cited in the Information Disclosure Statement filed December 31, 2003 (received January 2, 2004) only the English-language Abstracts have been considered because the documents are in Japanese.

However, Applicant directs the attention of the Examiner to MPEP 609 IIIA(3), which states in relevant part that “the requirement for a concise explanation of the relevance can be satisfied by submitting an English-language version of the search report or action which indicates the degree of relevance found by the foreign office.” Such an English-version was submitted with the IDS. Therefore, the Examiner is respectfully requested now to review and consider the references filed in the IDS filed December 31, 2003, and to acknowledge same.

Objections to the Drawings and to the Abstract

The Examiner objects to Figure 8 of the Drawings on the ground that a description of Reference Numeral S8 of Fig. 8 is missing in the Specification.

The portion of the Specification describing Figure 8 is amended. This amendment does not introduce impermissible new matter. Therefore, this objection should now be withdrawn.

Also, the Examiner objects to the Abstract of the Disclosure on the ground that the Abstract is too long.

The Abstract is amended. Therefore, this objection should now be withdrawn.

Rejection of Claims 1-6 under 35 U.S.C. § 112, Second Paragraph

Claims 1-6 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. This rejection is traversed.

(1) In claim 1, the Examiner states that the language “matches (at least) one of a predetermined instruction address and a predetermined instruction code” (underline added by Examiner) is unclear because it implies a disjunctive construction.

Applicant respectfully submits that the cited construction is standard in patent claims and widely used. Further, the meaning of the claim language is clear and unambiguous. Therefore, this portion of the rejection should now be withdrawn.

(2) The Examiner cites lines 23-25 of claim 1 and alleges that this language is unclear.

Applicant respectfully submits that the cited language is clear and unambiguous. However, in the interest of expediting prosecution of the Application, that portion of the claim is amended. Therefore, this portion of the rejection should now be withdrawn.

(3) In claims 4 and 5, the Examiner states that the language “and OR means” is unclear.

Applicant respectfully submits that the cited language is clear and unambiguous. The OR means (for example, not by way of limitation, OR gate, OR operator) are well known in the art. However, in the interest of expediting prosecution of the Application, that portion of the claim is amended by the inclusion of a comma. Therefore, the rejection should now be withdrawn with respect to claims 4 and 5.

(4) In claim 6, the Examiner alleges that the phrase cited is unclear.

Applicant respectfully submits that the cited language is clear and unambiguous. However, in the interest of expediting prosecution of the Application, that portion of the claim is amended. Therefore, this rejection should now be withdrawn with respect to claim 6.

Rejection of Claims 1-6 under 35 U.S.C. § 103

Claims 1-6 are rejected under 35 U.S.C. § 103 as being obvious from Swoboda, et al. U.S. Patent No. 5,535,331 and Craft, U.S. Patent No. 5,764,994. This rejection is traversed.

Among the problems recognized and solved by Applicant's claimed invention is that storing a full uncompressed instruction address only for a branch instruction is not always sufficient for a cost effective trace function and trace memory. In a programming development environment, a trace function stores an instruction address and an instruction code in a trace memory, so that execution results of the

computer program executed can later be analyzed for each instruction.¹ According to an aspect of Applicant's claimed invention, a full or uncompressed instruction address for an instruction code is stored in a trace memory not only for a branch instruction but also, for example, for a predetermined instruction other than a branch instruction. Accordingly, when a range or a section of a computer program is to be repeatedly traced (for example, because the program contains instructions in a "loop"), the section trace can be effectively accomplished.

For at least the following reasons, Applicant's claimed invention is neither anticipated by, nor obvious from, the cited prior art, including Swoboda and Craft. By way of example, independent claim 1 requires outputting a section trace start signal upon detecting that the instruction address/instruction code data matches a predetermined instruction code, and when the section trace starts signal is active, outputting the uncompressed instruction address as the trace data (the predetermined instruction code being different from a branch instruction). Further, independent claim 6 requires *inter alia*, upon detecting a predetermined instruction code, controlling to write an instruction address in the trace memory as uncompressed data (the predetermined instruction code being different from a branch instruction).

Swoboda discloses an integrated circuit condition sensing processor, in which operations of an integrated circuit are traced by detecting a jump address in the program counter sequence, and pushing the jump address onto a trace stack (Swoboda, Title and Abstract). Swoboda discloses a simulator that runs software to stimulate an

¹ The present discussion merely provides illustrative examples of Applicant's claimed invention. Applicant does not represent that every embodiment of Applicant's claimed invention necessarily embodies or provides the features or solutions herein discussed.

integrated circuit such that the chip can be developed and verified in a cost effective manner (Swoboda, col. 6, lines 42-64); emulation hardware and software to emulate a target chip during development and testing (Swoboda, col. 8, lines 13-27); and breakpoints in the software that allow program execution to be halted at specified instruction addresses (Swoboda, col. 9, lines 1-16).

The Examiner acknowledges that Swoboda does not disclose details related to the choice of compressing or not compressing certain data prior to storing (Paper No. 5, page 6). However, the Examiner alleges that Craft discloses these features. Craft discloses compressing compiled microcode to be executed within a data processing system (Craft, Abstract).

Craft discloses that executable microcode can be compressed by utilizing an address location of a branch instruction within a set of compiled microcode that is to be executed, and that each of the microcode segments is individually compressed by utilizing a data compression routine (Craft, col. 3, lines 15-45). Craft, Figure 2, also shows that after the locations of branch instructions within the microcode are identified, the address of branch locations are inserted for compressing or decompressing the microcode.

Craft does not disclose or suggest a program development apparatus as claimed in the independent claims 1 and 6. Further, Craft does not disclose or suggest a trace function or trace memory, as further required by independent claims 1 and 6.

In addition, independent claim 1 requires, *inter alia*, outputting a section trace start signal upon detecting that the instruction address/instruction code data matches a predetermined instruction code, and when the section trace starts signal is active,

outputting the uncompressed instruction address as the trace data. Further, independent claim 6 requires *inter alia*, upon detecting a predetermined instruction code, controlling to write an instruction address in the trace memory as uncompressed data. Craft and Swoboda, even taken together in combination of the whole,² do not disclose or suggest these features of independent claims 1 and 6.

In fact, Craft belongs to the prior art recognized by Applicant's disclosure, because Craft does not disclose or suggest the use of a predetermined instruction code in addition to the use of a branch instruction, as the basis for storing an uncompressed instruction address in trace memory. Craft and Swoboda do not disclose or suggest the problem recognized by Applicant's claimed invention, let alone provide the solutions recited in Applicant's independent claims 1 and 6.

Moreover, Craft may be said to teach away from Applicant's claimed invention as claimed in independent claims 1 and 6, because Craft teaches that the best strategy is to compress all in-line code sequences as one block of code regardless of the length, up to an unconditional or non-local branch point. (Craft, col. 3, lines 53-64). Therefore, the prior art including Swoboda and Craft, do not even remotely disclose or suggest the features of independent claims 1 and 6. Accordingly, it is respectfully submitted that Applicant's invention as claimed in independent claims 1 and 6 would not have been obvious to one of ordinary skill in the art from Swoboda and Craft.

Claims 2-5 depend from independent claim 1, and thus incorporate novel and nonobvious features thereof. Therefore, claims 2-5 are patentably distinguishable

² Applicant does not represent that such a combination of the references would have been obvious to one of ordinary skill.

over the prior art for at least the reasons that independent claim 1 is patentably distinguishable over the prior art. Accordingly, this rejection should now be withdrawn.

Filed herewith is a Petition for Extension of Time for a Three (3) month extension, with fee.

For at least the reasons set forth in the foregoing discussion, Applicant believes that the Application is now allowable, and respectfully requests that the Examiner reconsider the rejections and allow the Application. Should the Examiner have any questions regarding this Amendment, or regarding the Application generally, the Examiner is invited to telephone the undersigned attorney.

Respectfully submitted,



George Brieger
Registration No. 52,652

Scully, Scott, Murphy & Presser
400 Garden City Plaza
Garden City, New York 11530
(516) 742-4343 Ext. 503

GB:eg

Encl: Petition for Extension of Time for a three month extension, with fee.